REMARKS

As a preliminary matter, Applicants appreciate the Examiner's indication of allowable subject matter contained in claims 8 and 12-14.

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Dogliotti et al. (U.S. Patent No. 4,121,165). In response, Applicants traverse the rejection because the cited reference fails to disclose (or suggest) an optimum phase detection part that uses the output of an interpolation part to detect a phase error between an optimum point of a reproduced signal and a synchronization clock signal. Applicants also traverse the rejection because the cited reference fails to disclose a phase correction part that correct a phase of the reproduced signal based on the phase error, and an information data start detection part that detects start of information data based on the phase error.

FIG. 1 of Dogliotti shows a demodulator having a sampling and processing unit UCE that the Examiner equates to the interpolation part of the present invention. The outputs of the UCE are provided to a phase detector CJ, which the Examiner considers equivalent to the optimum phase detection part of the present invention. With respect to the phase corrector CJ, the Examiner asserts that there is a detection of a phase error between an optimum point of the reproduced signal and the synchronization clock signal by the phase corrector CJ. Applicants respectfully traverse this statement of the Examiner.

Dogliotti teaches the phase corrector CJ carries out the recovery of phase coherence on a baseband signal and emits, on a connection 3, a signal demodulated in a coherent way. (See col. 4, lns. 34-38). However, the phase corrector CJ is merely performing quadrature detection "from said in-phase and quadrature samples." (See col. 10, ln. 54).

The phase detector CJ is different from the present invention because there is no teaching in Dogliotti of detecting an optimum point of the reproduced signal. The phase detector CJ of Dogliotti does not detect a phase error between an optimum point of the reproduced signal and the synchronization clock signal. In Dogliotti, a synchronization estimator SS performs phase detection. However, the particular method of phase detection used by the synchronization estimator SS is not disclosed in Dogliotti. Dogliotti also fails to disclose any description of a reference pattern and an input to be compared therewith. Accordingly, Applicants respectfully submit that the method of phase detection used by Dogliotti is different from the cross-correlation method used in the present invention. Moreover, in Dogliotti, the time-base UT is considered to be the part that performs phase correction. However, both the synchronization estimator SS and the time-base UT are different in configuration from the optimum phase detection part and a phase correction part of the present invention. For at least these reasons, withdrawal of the §102 rejection of claim 1 is respectfully requested.

With respect to the phase correction part, Applicants respectfully submit that the phase detector CJ does not correct a phase of the reproduce signal using a phase

error that is determined based on an optimum point of the reproduce signal. That is, the phase of the reproduced signal is not corrected based on the phase error between the optimum point of the reproduce signal and the synchronization clock signal. For this additional reason, the rejection should be withdrawn.

Similarly, Dogliotti fails to disclose or suggest an information data start detection part that detects a start of information data based on the phase error detected by the optimum phase detection part. The Examiner asserts that Dogliotti teaches this feature in column 3, lines 64-68. However, the cited portion of Dogliotti merely shows that the synchronization estimator SS feeds back an error signal to a source of clock pulses. There is no disclosure in Dogliotti that a phase error between an optimum point of the reproduced signal and a synchronization clock signal is used by the synchronization estimator SS to detect a start of information data. For this reason, withdrawal of the §102 rejection is respectfully requested.

In addition to the above, Dogliotti is different from the present invention because Dogliotti uses a different method of sampling. Dogliotti has the synchronization estimator SS detect a phase error and a time base UT adjust the phase of a clock signal, gives an instruction on interpolating coefficients, and feeds CK2, CK3, and a signal IND to the sampling and processing unit UC. Accordingly, Dogliotti discloses a configuration that is a feedback configuration having an order of sampling as follows: detection, clock signal correction, and sampling.

In contrast, in one embodiment of the present invention, sampling is performed with a clock signal on which no phase correction is performed. Interpolation is performed on the sampled signal, and an interpolation signal having an optimum phase is selected based on a detected phase. Thus, the present application discloses a configuration that is a feed forward configuration without a loop, contrary to the feedback configuration of Dogliotti.

Furthermore, the Office Action states that the clock signals CK2 and CK3 shown in FIG. 2 of Dogliotti correspond to the "second clock signal having a frequency n times a frequency of the first clock signal." (See col. 3, lns. 29-37 of Dogliotti). In the cited portion of Dogliotti, timing signal CK1 has a cadence which is higher than a symbol frequency f_s, and the second and third timing signals CK2, CK3 have a cadence equaling that of the frequency f_s. Thus, the timing signals CK2, CK3 have a lower frequency (p/q) than the timing signal CK1.

In contrast, according to one embodiment of the present invention, a sampling clock signal and an interpolation clock signal are required to have a frequency equal to "n" times a clock signal for data reproduction (channel clock). For example, the A/D converter 106 of the present application samples a reproduced signal 131 based on the re-sampling clock signal RS_CLK 310 having a frequency "x" times the frequency of the synchronizing channel clock signal Ch. CLK 311, and the zero interpolation FIR filter 801 and the phase detector 802 operate based on a re-sampling clock signal RS_CLK 312 having a frequency "x" × "n" times the frequency of the synchronizing channel clock

signal Ch. CLK 311. Thus, the present invention is also different from Dogliotti because of this feature. (See Applicants' specification pg. 21, lns. 16-25). Accordingly, for all the reasons recited above, Applicants believe that Dogliotti does not disclose or suggest the optimum phase detection part, phase correction part, and information data start detection part of the present invention, and request withdrawal of the §102 rejection of claim 1.

Claims 2-7, 9-11, and 15-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Dogliotti and further in view of one or more of Lee (U.S. Patent No. 6,055,119), Tajiri et al. (U.S. Patent No. 5,946,359), and Kimoto et al. (U.S. Patent No. 4, 519,056). Applicants respectfully traverse these rejections.

Since claims 2-7, 9-11, and 15-17 ultimately depend upon claim 1, they necessarily include all of the features of independent claim 1 plus other additional features. Thus, Applicants submit that the §103 rejections of claims 2-7, 9-11, and 15-17 have also been overcome for the same reasons mentioned above to overcome the §102 rejection of independent claim 1, and also because the Lee, Tajiri and Kimoto references fail to overcome the deficiencies of Dogliotti, namely, detecting a phase error between an optimum point of a reproducing signal and a synchronization clock signal. Therefore, Applicants respectfully request that the §103 rejections of these claims also be withdrawn.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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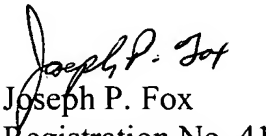
By 
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